WHAT IS CLAIMED IS:

1. A method of protecting an integrated circuit from over voltage, the method comprising:

accepting a voltage from a power supply input to the integrated circuit;

accepting a pad voltage from an external voltage source;

comparing the power supply voltage to a predetermined value; and

using the pad voltage to generate a bias voltage for the integrated circuit when the power supply is below the predetermined value.

2. A method as in claim 1 wherein the generation of the bias voltage comprises:

coupling the pad voltage into a drain of a PMOS (P-channel Metal Oxide Semiconductor) device; and

coupling the power supply voltage into a gate of the PMOS device.

3. A method as in claim 2 wherein using the pad voltage to generate a bias voltage for the integrated circuit further comprises:

coupling the drain of the PMOS device to the pad voltage; and

using the source voltage of the PMOS device to couple the pad voltage to the bias voltage.

4. A method as in claim 2 wherein coupling the pad voltage into the drain of a MOS (Metal Oxide Semiconductor) device comprises:

providing the pad voltage to an input of a plurality of diode connected MOS devices; and

coupling an output of the plurality of diode connected MOS devices to the drain of the MOS device.

5. A method for generating a bias voltage (bias_mid) from a pad voltage (Vpad), when a power supply (V_{DDO}) is not present the method comprising:

providing V_{DDO} to a first semiconductor device;

providing bias-mid to the first semiconductor device such that the first semiconductor device will turn off when bias_mid - V_{DDO} exceeds the threshold of the first semiconductor device; and

using the turn off of the first semiconductor device to couple Vpad to bias_mid.

6. The method of claim 5 wherein using the turn off of the first semiconductor device to couple Vpad to bias_mid further comprises:

turning on a second semiconductor device and turning off a third semiconductor device which are coupled together thereby providing a turn on voltage for a fourth semiconductor device; and

using the turn on of the fourth semiconductor device to couple Vpad to bias_mid.

7. A method for generating a voltage for biasing a device well, the method comprising:

providing a semiconductor device disposed between the device well and an input/output pad; and

turning on the semiconductor device when VDDO is lower than the pad voltage (Vpad), thereby coupling Vpad to the device well.

8. A method for generating a bias voltage (bias_mid) using a bias circuit the method comprising:

accepting an input/output circuit pad voltage (Vpad)from an input/output circuit pad;

accepting an output enable signal;

accepting a first input voltage V_{DDO};

accepting a second input voltage V_{DDP};

providing V_{DDP} voltage to Bias_Mid if the output enable signal is at an enable value; and

providing a voltage to bias mid that is proportional to the pad voltage if the output enable signal is at a disable value.

9. A method for generating a bias voltage (bias_mid) using a bias circuit the method comprising:

accepting an input/output circuit pad voltage (Vpad)from an input/output circuit pad;

accepting a power supply voltage (V_{DDO});

accepting a voltage V_{DDP};

providing a bias voltage to Bias_Mid, the bias voltage in a range having a maximum value of V_{DDP} + an offset voltage V_T and a minimum value of V_{DDO} - an offset voltage V_{TP}, if V_{DDO} is greater than a predetermined value; and

providing a bias voltage to Bias_Mid that is proportional to Vpad if V_{DDO} is not greater than a predetermined value.

10. A method as in claim 9 wherein V_{DDP} is equal to V_{DDO}.

11. A method for generating a bias voltage (bias_mid) using a bias circuit the method comprising:

accepting an input/output circuit pad voltage (Vpad)from an input/output circuit pad;

accepting a power supply voltage V_{DDO};

accepting a voltage V_{SSC};

providing a bias voltage to Bias_Mid, the bias voltage being in a range between $V_{SSC} + nV_T$ and $V_{DDO} - V_{TP}$ if V_{DDO} is greater than a predetermined value; and

providing a bias voltage to Bias_Mid, that is proportional to V_{PAD} if V_{DDO} is not greater than a predetermined value.

12. A method as in claim 11 wherein V_{SSC} is equal to zero volts.

13. A method for generating a bias voltage (bias_mid) using a bias circuit the method comprising:

accepting an input/output circuit pad voltage (Vpad) from an input/output circuit pad;

accepting a power supply voltage V_{DDO};

providing a voltage derived from V_{DDO} to Bias_Mid if V_{DDO} is greater than a predetermined value and providing a voltage derived from V_{PAD} to Bias_Mid if V_{DDO} is not greater than the predetermined value.

14. The method of claim 13 where the predetermined value is approximately 3.3 Volts.

15. A method for generating a bias voltage (bias_mid) using a bias circuit the method comprising:

accepting an input/output circuit pad voltage (Vpad) from an input/output circuit pad;

accepting a power supply voltage V_{DDO};

accepting a second voltage V_{DDP};

providing a voltage derived from V_{DDO} and V_{DDP} to Bias_Mid if V_{DDO} and V_{DDP} are greater than predetermined values; and

providing voltage derived from V_{PAD} to Bias_Mid if V_{DDO} and V_{DDP} are not greater than predetermined values.

16. A method for generating a bias voltage (bias_mid) using a bias circuit the method comprising:

accepting an input/output circuit pad voltage (Vpad)from an input/output circuit pad;

accepting a power supply voltage V_{DDO};

accepting a second voltage V_{DDP};

providing a voltage derived from V_{DDO} or V_{DDP} to Bias_Mid if V_{DDO} or V_{DDP} are greater than predetermined values; and providing voltage derived from V_{PAD} to Bias_Mid if V_{DDO} and V_{DDP} are not greater than predetermined values.

17. An apparatus for providing an input output from an integrated circuit, the apparatus comprising:

an input/output (I/O) pad;

an upper pair of P-channel Metal Oxide Semiconductor (PMOS) devices, a first of the upper PMOS devices having source coupled to a power supply (V_{DDO})and drain coupled to source of a second upper PMOS device, the second PMOS device having drain coupled to the I/O pad;

a lower pair of N-channel MOS devices (NMOS), a first of the upper NMOS devices having a drain coupled to the I/O pad and a source coupled to a drain of a second lower NMOS device, the second NMOS device having a source coupled to a ground potential;

a first bias circuit coupled to a gate of the first upper PMOS device, said bias circuit providing a first bias voltage to the gate of the first upper PMOS device when the I/O pad is in an output mode and V_{DDO} voltage otherwise;

a second bias circuit coupled to a gate of the second lower NMOS device, said bias circuit providing a second bias

voltage to the gate of the second lower NMOS device when the I/O pad is in an output mode and a ground voltage otherwise;

a third bias circuit coupled to a gate of the second upper PMOS device, said bias circuit providing a third bias voltage to the gate of the second upper MOS device; and

a fourth bias circuit coupled to a gate of the first lower NMOS device, said bias circuit providing a fourth bias voltage to the gate of the first lower MOS device, said fourth bias voltage in a range having a maximum value of $V_{SSC} + nV_T$, and a minimum value of $V_{DDO} - V_{Tp}$, when V_{DDO} is greater than a predetermined value, and wherein nV_T and V_{Tp} are offset voltages, and when V_{DDO} is not greater than a predetermined value the fourth bias voltage is derived from the pad voltage;

18. An apparatus as in claim 17 wherein VSSC is equal to ground potential.

19. An apparatus as in claim 17 wherein nV_T and V_{Tp} are the same.

20. An apparatus for providing an input output from an integrated circuit, the apparatus comprising:

an input/output (I/O) pad;

an upper pair of P-channel Metal Oxide Semiconductor (PMOS) devices, a first of the upper PMOS devices having source coupled to a power supply (V_{DDO})and drain coupled to source of a second upper PMOS device, the second PMOS device having drain coupled to the I/O pad;

a lower pair of N-channel MOS devices (NMOS), a first of the upper NMOS devices having a drain coupled to the I/O pad and a source coupled to a drain of a second lower NMOS device, the second NMOS device having a source coupled to a ground potential;

a first bias circuit coupled to a gate of the first upper PMOS device, said bias circuit providing a first bias voltage to the gate of the first upper PMOS device when the I/O pad is in an output mode and V_{DDO} voltage otherwise;

a second bias circuit coupled to a gate of the second lower NMOS device, said bias circuit providing a second bias voltage to the gate of the second lower NMOS device when the I/O pad is in an output mode and a ground voltage otherwise;

a third bias circuit coupled to a gate of the second upper PMOS device, said bias circuit providing a third bias voltage to the gate of the second upper MOS device; and

a fourth bias circuit coupled to a gate of the first lower NMOS device, said bias circuit providing a fourth bias voltage to the gate of the first lower MOS device depending on the voltage on the I/O pad (V_{PAD}), and wherein the fourth bias voltage is in a range having a maximum value of $V_{DDO} + V_{Tp}$ and a minimum value of $V_{DDO} - V_{TP}$ when V_{DDO} is greater than a predetermined value, where V_T and V_{Tp} are offset voltages.

21. An apparatus as in claim 20 wherein V_{SSC} is at ground potential.

22. An apparatus as in claim 20 wherein V_T and V_{Tp} are the same offset voltages.